Warren P. Waters
2721 Windover Drive
Corona del Mar, CA
714/760-9580

EDUCATION:

California Institute of Technology
Degree: B.S. Applied Physics, June 1949

University of Southern California
Degree: M.S. Physics, June 1954 (Course work completed for PhD).

MILITARY SERVICE: U.S. Army 1942-1946; Combat Infantry Badge, Bronze Star, Purple Heart

PROFESSIONAL EXPERIENCE:

January 1971 - October 1971
MONITRON INDUSTRIES, INC.; Huntington Beach
Position: Microelectronics Consultant

Projects included:
1) Development of low cost thick, film hybrid I.C. body temperature transducer-R.F. Transmitter.
2) Developed techniques for adjusting thermal calibration and R.F. bandwidth.
3) Analysis of automatic assembly techniques and production costs.

December 1969 - November 1970
TELEDYNE SEMICONDUCTOR; Hawthorne
Position: Manager - Transistor Research & Development

Projects included:
1) Development of a back contact for high speed die mounting without scrubbing.
2) Development of 2-micrometer finger, microwave transistors using overlay Si_2N_4-SiO_2 layers.
3) Set up 50-amp power transistor pilot production.
4) Development of an analog circuit to plot epitaxial layer profile by probing a diode.
5) Development of a radiation-tolerant transistor, some of which showed flat hFE characteristics from 250°C down to 77°K.
6) Process improvement to minimize beta drop at low current levels.

November 1967 - December 1969
ELECTRONIC RESOURCES, INC.; Div. Tasker Industries, Whittaker Corp.
Los Angeles, CA
Position: Manager - Microelectronic Laboratory

Responsibilities included:
1) Designing laboratory and setting up facility.
2) Establishing hybrid thin-film technology for in-house microcircuit prototypes.
3) Developing microstrip technology for microwave microelectronic assembly.
4) Setting up module fabrication technology for multi-chip subsystem assembly.

RESUME

NAME: Warren P. Waters

TITLE: Engineer/Scientist V

EDUCATION: M.S. Physics, USC, 1954
B.S., Applied Physics, California Institute of Technology, 1949

ROCKWELL EXPERIENCE:

2/80 to 12/81 -- Custom MOS/Custom Device Products, Newport Beach

- Converted Kasper 2000 Aligners to vacuum chuck operation to minimize oxygen desensitization of negative resist.
- Modified gate oxidation and implant-anneal tubes to minimize interface charge from oxygen backstreaming.
- Use Suprem II on TSO for computer simulation of current processes and for evaluation and establishment of process parameters prior to running on the line. Have also used ROTM 3 and other device modeling programs.
- Instituted and currently operate system for computer input of weekly wafer map and probe data. Will provide tab runs of histograms on map and probe data and parameter trend charts. Correlations between any parameters including probe yields can be plotted on computer files of data back into 1980.
- Evaluated process improvement using 1000 Å CVD undensified oxide layers applied on top of the 2-micrometer thick field oxide. This provides accurately controlled undercutting to give a uniformly tapered slope to the etched window. This will practically eliminate step-coverage problems.
- Have recently been able to adjust enhancement and depletion implants to improve probe yields on double implant processes.
- Currently evaluating C/V analysis of doping levels under gate oxides. In correlation with drain breakdowns increased doping of the channel is indicated toward the flat of the wafers placed "up" in all furnaces. This can account for increased high V_gst map values toward the wafer flats.

11/71 - 2/80 -- CTD Department/Microelectronic R & D Center

- Originally hired as MTS V working on a CTD optical programmable, non-volatile memory array concept using Si_3N_4/SiO_2 interface storage.
- Set up operational four-phase CTD processes, as follows:
  a) with double Al metal gates,
  b) with double In_2O_3/SnO_2 transparent, conducting gates. This was the first practical high-resolution photoresist process for ITO gates,
  c) double-poly, hi-resolution, hi-conduction gates,
  d) buried-channel CTD's with EPI and diffused channel P-N junctions.

ROCKWELL EXPERIENCE, continued:

- Transferred the CTD's developed and processes to Military MOS pilot line.
- Ordered early Canon FPA-121 projection aligner for 2" wafers with option to trade in for 3" model. Traded in for only existing Rockwell FPA-121 3" wafer aligner.
- Became lead scientist responsible for CTD processing. Set up and staffed new CTD processing lab with all equipment capable of conversion to 3" wafers.
- Used Canon aligners to process CTD's consistently with 2-micrometer gates and spacings with good overlap alignment of second layer. 1.5 micrometer gates and spacings were made with some alignment difficulties. Experimental test patterns were defined to 1.2 micrometer lines and space.
- Member of Rockwell committee for initiating five year program on Fine-Line Photo Lithography. Reported on BTL system using E-Beam defined Au layers to expose wafers with soft X-rays.
- Given Staff Scientist job-title in CTD organization.
- On committee to review and select VHSIC stepped wafer exposure systems.
- Invented patentable and practical high resolution CTD ROM with a discretionary final Al top layer to define the memory pattern. No CTD ROM structure has been found in the literature to date. The ROM CTD was required for a system proposal.
- Applied Suprem I and II to CTD process optimization.
- Project responsibility on development of a very high resolution charge sensor array. This used a "fill and spill" input CTD structure where the open gate controlled the "spilled" charge transferred, by the amount of external charge sensed over the gate window. Personally fabricated glass pedestals with less than 0.010" diameter flat surface and 0.012" high coated with In_2O_3-SnO_2 for charge-probing the sensor area. This flat surface was aligned to the gate area by a 40X microscope objective looking up through the pedestal itself from below. Set up test equipment and measured outputs.
- Set up C/T techniques for bulk lifetime evaluation. Used this to evaluate successful experiments for high energy Argon implant gettering for lifetime improvement.

PRE-ROCKWELL EXPERIENCE:

See attached information.

PROFESSIONAL EXPERIENCE, continued:

5) Developing electroforming techniques for fabricating low loss antennas, filters and inductors on ceramic substrates.
6) Built high power, high efficiency prototype RF jammer on BeO substrate.
7) Applied course on computer device simulation to optimize coupling circuits for RF jammer.

January 1967 - November 1967
HUGHES AIRCRAFT COMPANY, Microelectronics Division; Newport Beach
Position: Assistant Manager - Microelectronics Laboratory

Programs included:
1) Thin film hybrid pilot line for in-house and external customers.
2) Thin film passive element R&D for high sheet resistivities.
3) Custom monolithic circuit fabrication. This included use of substrate PNP transistors and buried layers.
4) Development of new flip-chip glass ambient transistors (2N918).
5) Flip-chip ultrasonic bonding technology for monolithic circuits. This included applying "bump" technology to substrates and extending the contact pattern on the monolithic circuits over a glass layer. Patent now issued.
6) Development of metallurgy for the heat removal from the emitter side of an "overlay" power transistor structure. Obtained 40% reduction in thermal resistance with conducting clip on back side.
7) Development of 1-micron resolution photomask equipment for experimental high frequency devices.

February 1966 - January 1967
HUGHES AIRCRAFT COMPANY, Solid State Research Center; Newport Beach
Position: Manager - Solid State Research Center
Reporting: Directly to the Vice President and Director of Hughes Research Laboratories; Malibu, CA

Three program managers covered the following areas:

Program I. Advanced Devices
1) Silicon on sapphire MOS and bipolar transistors, including structures for radiation effect studies.
2) Silicon on sapphire thin film gate circuit.
3) Space-charge-limited-triode development, made silicon on sapphire for low noise amplifier.
4) Multi-channel FET development. Target 5W at 100 mHz.

Program II. Microwave Devices
1) Au bonded Si Schottky barrier low noise mixer diodes for Surveyor.
2) Planar Schottky barrier diode development.
3) PIN avalanche diode development for power at microwave frequencies.
4) Ag bonded Ge varactor diodes.
5) Photon coupler, GaAs-Si diode with 14 KV isolation.

PROFESSIONAL EXPERIENCE, continued:

Program III. Microelectronic Technology
1) 14 Bump flip chip monolithic circuits.
2) Array fabrication with glass applied to available monolithic circuit slices.
3) Micro-circuit and silicon power transistor fabrication for radiation effect studies.
4) Si_3N_4 MISFET transistor developed for radiation effect evaluation.
5) Pilot production of low 1/f noise MOSFET transistors.
6) Tetrode MOSFET developed for high voltage operation.
7) Pt and Ti silicide metallurgy developed for improved ohmic contacts to device structures.
8) MOSFET studies included invention of Si gate by Program Manager, Hans Dill.

June 1962 - January 1966
TEXAS INSTRUMENTS, Semiconductor-Components Division; Dallas, TX
Position: Manager - Exploratory Development; Semiconductor Research and Development Laboratory

1965 projects at Texas Instruments included responsibilities for:
1) Very high resolution photoresist and diffusion techniques for fabrication of 2.5 GHz, 2W transistors for the MERA contracts.
2) Strip-line ceramic circuits for operation up to 10 GHz with included solid state elements for MERA modules.
3) Si and GaAs planar Schottky barrier diodes for microwave mixers and varactors.
4) Low noise planar Ge transistors for operation up to and including 3 Ghz.
5) Vapor deposition of SiO_2 and Al_2O_3 layers for diffusion masking and junction "passivation".

Previous projects at Texas Instruments included responsibilities for:
1) Fabrication of networks with sub-epitaxial (buried layers) deposition for low collector series resistance.
2) Planar Ge tunnel diodes for fast switching applications.
3) Development of GaAs mesa transistors.
4) Co-axial and "TI-line" packages for operation above 1 GHz.
5) Development of high resolution (0.1 mil stripes and spacing) Si transistors for operation above 1 GHz.

June 1952 - March 1962
HUGHES AIRCRAFT COMPANY, Semiconductor Division; Newport Beach
Position: Manager - Device Development Department

Projects included:
1) High "Q" tunable solid-state inductance.
2) Gold-bonded Si switching diodes (0.5 nanoseconds).
3) Au and Ag-bonded Ge and Si mesa High "Q" varactor diodes.
4) Post-alloy diffused Ge and GaAs transistors.
5) Si P-N junction particle detectors.
6) PNP silicon alloy transistor development. Patents issued.
7) Early development of Ge NPN alloy transistors.
8) Co-axial transistor package. Patent issued.

ADDITIONAL EXPERIENCE:

Spring Term - 1967
Local Co-ordinator Microelectronics Lecture Series.

Fall Term - 1957
University of California at Los Angeles
University Extension Course
Lecturer - "Transistor Electronics" XL 198

Fall and Spring Terms - 1951-1952
University of Southern California
Physics Department, University Park
Los Angeles, CA
Research Assistant - O.N.R. Contract

1949-1950 - University of California Scientific Labs
Los Alamos, NM
Research Assistant - 12 MEV Van de Graff Accellerator Group P-9.

Summers - 1947-1948
University of California Scientific Labs
Los Alamos, NM
Research Assistant - Electronics Group P-1.

PROFESSIONAL AFFILIATIONS:

Member - American Physical Society; 1951-1972

Senior Member - Institute of Electrical and Electronic Engineers

Member - Electron Devices Group

Member - Microwave Theory and Techniques Group; 1967-1970

Member - Electrochemical Society

PUBLICATIONS:

Numerous papers presented and published in the semiconductor field. Seven patents issued on semiconductor device structures and processes with three applications currently pending.

WARREN P. WATERS
2721 Windover Drive
Corona del Mar, CA
(714) 760-9580

TITLE: Staff Process Engineer V

EDUCATION: M.S. Physics, USC Graduate School, 1954
B.S. Applied Physics California Institute of Technology, 1949

CLEARANCES: Secret,"Q" and many others

RECENT ROCKWELL EXPERIENCE: Semiconductor Products Division, Newport Beach

12/81 to 4/85 -- Processes

- Participated in First CMOS Process established in Newport Beach
- Expedited 65C02 Microprocessor - First CMOS circuit in Newport Beach.
- Input and debugged first lot followers in PROMIS CAM system.
- Added device specified parameters to lot followers.
- Only Process Engineer in Fab area on weekend shift. Monitored all equipment and all CMOS, CEMOS, and NMOS processes down to 2 um line widths
- Received highest cost improvement award in Fab IV for 1983.

Photo Processes

- Set up Perkin-Elmer 241 and 341 auto aligners in Fab IV. Established auto align target placements on masks and experimentally determined optimum polarity and line widths for each layer wafer targets.
- Also evolved special cross-alignment verniers to check alignment accuracy of alternate layers to the ones aligned by the PE 241.
- Set up special puddle development used to open contact windows consistently.
- Obtained fusion deep U.V. system for photoresist profile hardening.

Resume, Warren P. Waters

RECENT ROCKWELL EXPERIENCE, continued:

Plasma Deposition

- Deposited $Si_3 N_4$ overcoats using ASM PECVD equipment with limited depletion mode R.F. power.
- Also depositions of $Si_x O_y N_z$ to controlled index to permit U.V. transmission in overcoats on EMOS memory chips.
- Set up ASM 200 mm PECVD system for depositing 7% Phos oxides, $Si_3 N_4$, $Si_x O_y N_z$ and Boro-Phospho-Silicant glass.
- Stored programs in Supervisor. Computer soft contact boat loader updated with home position for loading and unloading wafers.
- Worked out dry annealing process for BPSG depositions. Obtained smooth slopes annealing at $875^{o}C$.
- Made SEM sections showing BPSG layer profiles and double poly lines without etching.